WHAT IS CLAIMED IS:

1. A sigma-delta modulator, comprising:

a lower-order accumulator chain configured to process only lower-order bits of an input number;

a higher-order accumulator chain configured to process only higher-order bits of said input number; and

a combiner coupled to both said lower-order and higher-order accumulator chains and configured to align results therefrom to generate output bits of a given order.

2. The sigma-delta modulator as recited in Claim 1 wherein said lower-order bits equal in number said higher-order bits.

3. The sigma-delta modulator as recited in Claim 1 wherein accumulators in said lower-order accumulator chain equal in number both accumulators in said higher-order accumulator chain and said given order.

4. The sigma-delta modulator as recited in Claim 1 wherein said higher-order accumulator chain has pre-accumulator delay logic associated therewith.

5. The sigma-delta modulator as recited in Claim 1 wherein said lower-order accumulator chain and said higher-order accumulator chain have inter-accumulator delay logic associated therewith.

6. The sigma-delta modulator as recited in Claim 1 further comprising at least one other accumulator chain.

7. The sigma-delta modulator as recited in Claim 1 wherein said lower-order accumulator chain and said higher-order accumulator chain are embodied in a deep-submicron complementary metal-oxide semiconductor integrated circuit.

8. The sigma-delta modulator as recited in Claim 1 wherein said lower-order accumulator chain and said higher-order accumulator chain have multiple stages and each of said multiple stages is controlled by an unique reset signal.

9. A method of performing sigma-delta modulation, comprising:

processing only lower-order bits of an input number in a lower-order accumulator chain;

processing only higher-order bits of said input number in a higher-order accumulator chain; and

aligning results from both said lower-order and higher-order accumulator chains to generate output bits of a given order.

10. The method as recited in Claim 9 wherein said lower-order bits equal in number said higher-order bits.

11. The method as recited in Claim 9 wherein accumulators in said lower-order accumulator chain equal in number both accumulators in said higher-order accumulator chain and said given order.

12. The method as recited in Claim 9 wherein said higher-order accumulator chain has pre-accumulator delay logic associated therewith.

13. The method as recited in Claim 9 wherein said lower-order accumulator chain and said higher-order accumulator chain have inter-accumulator delay logic associated therewith.

14. The method as recited in Claim 9 further comprising processing other bits of said input number in at least one other accumulator chain.

15. The method as recited in Claim 9 wherein said lower-order accumulator chain and said higher-order accumulator chain are embodied in a deep-submicron complementary metal-oxide semiconductor integrated circuit.

16. The method as recited in Claim 9 wherein said lower-order accumulator chain and said higher-order accumulator chain have multiple stages and said method further comprises controlling each of said multiple stages by an unique reset signal.

17. An digital-to-analog converter, comprising:

digital circuitry configured to provide input numbers from a digital input;

a sigma-delta modulator coupled to said digital circuitry and including:

a lower-order accumulator chain that processes only lower-order bits of said input numbers,

a higher-order accumulator chain that processes only higher-order bits of said input numbers, and

a combiner, coupled to both said lower-order and higher-order accumulator chains, that aligns results therefrom to generate output bits of a given order; and

a digital-to-continuous converter, coupled to said sigma-delta modulator, that converts said output bits into a continuous domain.

18. The digital-to-analog converter as recited in Claim 17 wherein said sigma-delta modulator is a multistage noise shaping (MASH) sigma-delta modulator.

19. The digital-to-analog converter as recited in Claim 17 wherein said input digital circuitry includes an upsampler or an interpolator.

20. The digital-to-analog converter as recited in Claim 17 wherein said lower-order bits equal in number said higher-order bits.

21. The digital-to-analog converter as recited in Claim 17 wherein accumulators in said lower-order accumulator chain equal in number both accumulators in said higher-order accumulator chain and said given order.

22. The digital-to-analog converter as recited in Claim 17 wherein said higher-order accumulator chain has pre-accumulator delay logic associated therewith.

23. The digital-to-analog converter as recited in Claim 18 wherein said lower-order accumulator chain and said higher-order accumulator chain have inter-accumulator delay logic associated therewith.

24. The digital-to-analog converter as recited in Claim 17 further comprising at least one other accumulator chain.

25. The digital-to-analog converter as recited in Claim 17 wherein said lower-order accumulator chain and said higher-order accumulator chain are embodied in a deep-submicron complementary metal-oxide semiconductor integrated circuit.

26. The digital-to-analog converter as recited in Claim 17 wherein said lower-order accumulator chain and said higher-order accumulator chain have multiple stages and each of said multiple stages is controlled by an unique reset signal.

27. The digital-to-analog converter as recited in Claim 17 wherein said digital-to-continuous converter includes a digitally-controlled RF power amplifier and said digital-to-analog converter is a digital-to-RF amplitude converter.

28. The digital-to-analog converter as recited in Claim 17 wherein said generated output bits are in a unit-weighted format and said digital-to-continuous converter employs a unit-weighted element for processing thereof.